Integrated Circuits for a Display Array

Abstract of the Disclosure

A device for use in a display system comprising an array of pixel cells formed on a substrate. Each pixel cell is coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate. The device comprises first and second transistors formed on said substrate. Each transistor has a gate electrode and first and second electrodes defining a serpentine channel region there between. Voltage applied to the gate electrode controls conductivity of the channel region. Preferably, the a common electrode comprises one of the first and second electrodes of said first transistor and one of said first and second electrodes of said second transistor. The first and second transistors are preferably coupled between a gate line (or data line) and respective probe pads formed on the substrate and selectively couple the respective probe pad to the gate line (or data line) during a test routine whereby charge is written to, stored, and read from the array of pixel cells.